AMENDMENTS IN THE DRAWINGS:

Formal drawings are submitted herewith. The formal drawings include amendments to Figures 2, 3g, 3h, 3i, 3j, 3k, 3l, 4d, 4e and 4f. To avoid confusion caused by the duplicate use of reference numbers 70 and 72, steps 68, 70 and 72 in Fig. 2 have been relabeled 67, 68 and 69, respectively. In Figures 3g, 3h, 3i, 3j, 3k, 3l, 4d, 4e and 4f, the reference numeral corresponding to the backgate has been changed from "22" to "94". In Figures 3j, 3k, 3l and 4f, the reference numeral corresponding to the channel region has been changed from "84" to "92". In Figures 3g and 4d, the reference numeral corresponding to the backgate region has been changed from "84" to "84a". In Figure 3i, the reference numeral 80 and corresponding reference line has been moved to properly reference feature 80. No new matter has been added.

Attachment: Seven Replacement Sheets

AMENDMENTS IN THE SPECIFICATION:

In the Specification:

Please replace the paragraph beginning at page 6, line 20, with the following rewritten paragraph:

The active region 12 is isolated by an insulating trench 20 which extends from the surface 21 of the silicon device layer ~~32~~ 26 down to the insulating layer 28. The insulating trench 20 has side walls 22 which define the perimeter 24 of the active region 12 and function to isolate the active region 12 from other structures formed in the silicon device layer ~~32~~ 26.

Please replace the paragraph beginning at page 6, line 32, with the following rewritten paragraph:

In the exemplary embodiment, FET 10 is a normally "off" FET wherein when the potential on the silicon carbide gate 34 and the silicon carbide ~~back-gate~~ backgate 38 is at ground, no current will flow from the source region 16 to the drain region 18 because a depletion on the upper portion of the central channel region 14 caused by the silicon carbide gate 34 will extend towards a depletion region on the lower portion of the central channel region 14 caused by the silicon carbide backgate 38. The two depletion regions will "pinch-off" current flow between the source region 16 and the drain region 18.

Please replace the paragraph beginning at page 7, line 16, with the following rewritten paragraph:

It should be appreciated that carbon, having an energy gap greater than silicon, tends to increase minority carriers (e.g. free electrons) within the P-type ~~silicon carbide~~ silicon carbide gate 34 and silicon carbide backgate 38. As such, junction capacitance at the heterojunctions formed between the channel region 14 and the silicon carbide gate 34 and the silicon carbide backgate 38 is increased. The increased junction capacitance tends to

increase the thickness of the depletion regions within the central channel region 14 without increasing the charge that diffuses from the channel region 14 into the silicon carbide gate 34 and the silicon carbide backgate 38.

Please replace the paragraph beginning at page 9, line 15, with the following rewritten paragraph:

Step 54 represents etching a backgate trench 84 into the central portion of the island 80 to the depth of the buried oxide layer ~~84~~ 72 as shown in Figure 3d. The etching step 54 again includes growing a thin oxide layer 86 on the surface of the wafer and forming a silicon nitride mask 88 to define and expose the area corresponding to the backgate trench 84. Once the mask 88 is formed, an anisotropic etch with a etching compound such as hydrogen bromide (Hbr) is preferably used to etch the backgate trench 84 in the region of the island 80 not masked by the silicon nitride mask 88.

Please replace the paragraph beginning at page 10, line 4, with the following rewritten paragraph:

Step 60 represents etching the channel region 92 into the backgate region ~~84~~ 84a to the depth effective to leave a backgate ~~22~~ 94 above the buried oxide layer 72 as is shown in Figure 3g and Figure 4d. It should also be appreciated that the channel region 92 does not extend into the region 91 such that region 91 is the same silicon carbide material as backgate 94.

Please replace the paragraph beginning at page 10, line 20, with the following rewritten paragraph:

Step 66 represents lightly implanting the channel region ~~84~~ 92 with a donor impurity such as Arsenic to increase electron conductivity as is shown in Figure 3i.

Please replace the paragraph beginning at page 10, line 23, with the following rewritten paragraph:

Step ~~68~~ 67 represents forming the gate 34 on the top of the channel region ~~84~~ 92. More specifically, a silicon carbide layer is deposited on the surface of the channel region ~~84~~ 92 and is patterned and etched to form the gate 34 as is shown in Figure 3j. The silicon carbide may be deposited using low pressure chemical vapor deposition (LPCVD) as is known by those skilled in the art and etched utilizing the above described photolithography techniques. At step ~~70~~ 68, the source region 16 and drain region 18 on opposing sides of the central channel region ~~84~~ 92 may be implanted with an donor impurity such as arsenic as is shown in Figure 3k. Thereafter, the mask over the gate 34 is removed yielding the FET 10 structure of Figure 1 as is shown in cross section in Figure 3l and Figure 4f.